

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. : DIVISIONAL APPLICATION OF 09/982,413  
Applicant : Kianian et al.  
Filed : February 10, 2004  
TC/A.U. : Unknown  
Examiner : Unknown  
Title : SELF ALIGNED METHOD OF FORMING A  
SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE  
MEMORY CELLS WITH BURIED BIT-LINE AND VERTICAL  
WORD LINE TRANSISTOR (as amended herein)  
Docket No. : 2102397-992011  
Customer No. : 26379

EXPRESS MAIL NUMBER: EV 302280099 US

DATE OF DEPOSIT: February 10, 2004

I hereby certify that this paper is being deposited with  
the United States Postal Service "EXPRESS MAIL  
Post Office to Addressee" service under 37 CFR 1.10  
on the date indicated above and is addressed to: Mail  
Stop Patent Application, Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

By: \_\_\_\_\_

SUSAN PINGUE

PRELIMINARY AMENDMENT

Sir:

Prior to examination of the above-identified application, which is a divisional of  
application serial number 09/982,413 filed on October 17, 2001, please amend the application as  
follows:

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this  
paper.

**Remarks/Arguments** begin on page 9 of this paper.